REMARKS

Claims 55-84 remain in this application. Claims 1, 3-14, 16-19, 21-24, and 31-54 have been cancelled without prejudice. Claims 55-84 have been added. The new claims are fully disclosed and supported in the original specification and no new matter has been added. The Applicants respectfully request reconsideration of this application as amended.

Title

Applicants have amended the title of the invention.

Specification

Applicants submit herein proposed amendments to correct informalities. These amendments add no new matter.

Conclusion

The new claims are believed to distinguish over the cited art and be in condition for allowance. The Examiner is requested to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: December 5, 2002

Brent E. Vecchia

Brent E. Vecchia
Reg. No. 48,011

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1030
(303) 740-1980

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Title:

The title has been amended as follows:

[A Method and Apparatus For] Testing a Bus Using Bus Specific Instructions

In The Specification:

The paragraph beginning at page 8, line 10 has been amended as follows:

--A similar problem occurs in the development of components such as chipsets and processors. In the early design stages, the components being developed are simulated in a software environment and are often driven by a high-level bus model known in the art as a bus functional model (BFM). A simulation stimulus software language may then be used to exercise the simulated system. While these methods provide a designer a high level of control, observability and repeatability when testing system designs, the simulation environments are extremely slow, typically operating at about 1-10 Hz. Further, there is no corresponding capability for repeating the simulation on actual systems (hardware) during the design stages that provides the desired control, observability, and repeatability.--

The paragraph beginning at page 15, line 14 has been amended as follows:

--The host computer 80 provides a programming and control interface to the transaction generator 20. In addition to providing the binary object file 84 containing the instructions to the instruction memory of the transaction generator 20, the host computer 80 programs the various logic devices in the transaction generator using standard software packages available for this purpose. Further, the host computer 80 may exchange data with the data memory of the transaction generator [80] 20, and provide the

proper responses to received bus signals to the transaction generator [80] 20 response memory. Alternatively, the transaction generator 20 may be implemented without requiring a host computer 80. The transaction generator 20 may be configured such that necessary programming and control is provided by the system with which it is implemented. In other words, the processor(s) 70 coupled to the processor bus 26, along with the associated control and memory devices 72, 74 coupled to the system bus and other system components (not shown) coupled to the I/O bus 76, may provide the programming and control functions of the host computer. --

In The Claims:

Claim 1 has been cancelled.

Claims 3-14 have been cancelled.

Claims 16-19 have been cancelled.

Claims 21-24 have been cancelled.

Claims 31 – 54 have been cancelled.

Claims 55-84 are new.